Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3105511	memory or storage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:28
L2	44976	1 and cell with (bit adj line or bitline or digit adj line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:47
L3	16	2 and cell with source near3 (connect$5 or coupl$5 or receiv$5) near3 control adj signal	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:34
L4	5	3 and (dynamic or dram)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:34
L5	21077	2 and (dram or dynamic)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:47
L6	220	5 and floating adj body	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:48
L7	25	5 and floating adj body adj transistor	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:48

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3105511	memory or storage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:28
L2	44976	1 and cell with (bit adj line or bitline or digit adj line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:47
L3	16	2 and cell with source near3 (connect$5 or coupl$5 or receiv$5) near3 control adj signal	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:34
L4	5	3 and (dynamic or dram)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:34
L5	21077	2 and (dram or dynamic)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:47
L6	220	5 and floating adj body	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 19:48
L7	25	5 and floating adj body adj transistor	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 20:57
L8	3	6 and reset$5 with floating adj body	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 20:52
L11	39	6 and writ$5 with floating adj body	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 20:53
L12	6	11 and reset$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 20:55
L13	0	6 and reset$6 with floating adj body with overlap$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 20:56
L14	10	7 and processor	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:10

L15	848	2 and off near2 chip	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:13
L16	113	2 and off near2 chip with (cache or chip adj set or graphic interface)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:15
L17	1	16 and memory near processor with chip	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:14
L18	57	2 and off near2 chip with (cache or chip adj set or graphic adj interface)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:16
L19	0	17 and 18	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:16
L20	55	2 and off-chip with (cache or chip adj set or graphic adj interface)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:19
L21	0	20 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:16
L22	8	2 and off-die with (cache or chip adj set or graphic adj interface)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:28
L23	15	2 and purge adj line	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/05/12 21:28